REMARKS/ARGUMENTS

Claims 1-21 are pending in the application. Reconsideration in view the following remarks is respectfully requested. The Office Action also rejects claims 1-21 under 35 U.S.C. 103(a) as being unpatentable over Parady (U.S. Patent No. 5,933,627) in view of Hennessy (Computer Organization and Design).

Applicants respectfully submit that none of the cited sections of Parady teach, suggest or reflect at least "[a] method of handling operations in a multi-threaded processing system, comprising determining if a stalled operation of a first thread is due to a loading of data from a memory device and flushing an instruction from said first thread from a pipeline of said processing system when data is to be loaded from said memory device before executing said instruction" [as in claim 1].

The Office Action states, in essence –

> Parady does not disclose flushing an instruction from said first thread from a pipeline of said processing system when data is to be loaded from said memory device before executing said instruction. Hennessy has shown flushing an instruction from a pipeline of said processing system. Page 505 of Hennessy shows that flushing is done in various pipeline stages to get rid of invalid instructions on a transfer of control such as an exception or branch or transfer of control to another thread as is the case in Parady as shown above. Page 505 of Hennessy shows that transferring control (such as from one thread to another in the case of Parady) immediately (by flushing) is desirable so that invalid values (from invalid instructions) do not contaminate registers or memory locations. This ability to not contaminate registers and memory would have motivated one of ordinary skill in the art to modify the design of Parady to flush instructions on a transfer of control as taught by Hennessy. With this modification in place, Parady would flush instructions stored in the dispatch unit (column 3, lines 12-14 show that this unit holds up to four decoded instructions for execution) so they are not advanced for execution and contaminate memory and registers, as described by Hennessy, when Parady switches (transfers) to another flow of control of thread. Parady has further shown in column 4, lines 45-51 an embodiment where control is immediately transferred back to the thread that executed a load when the data is ready before other threads can advance. This means that an instruction about to be dispatched would have been flushed instruction can execute. It would have been obvious to one of ordinary skill in the art to modify the design of Parady to use the flushing technique described by Hennessy so that instructions not in the flow of control after a thread switch do not contaminate register and memory values.

Applicants respectfully submit that the cited references fail to teach, suggest or disclose "...flushing an instruction from said first thread from a pipeline of said processing system *when data is to be loaded from said memory device before executing said instruction"* as recited in claim 1. Neither the cited references Parady or Hennessy, nor the Office Action

address at least the limitation of flushing an instruction when data is to be loaded from said memory device before executing said instruction. Support for this limitation can be found at page 5 line 22 which states:

> An example of the operation of pipeline control logic 107 in this embodiment is shown in Fig. 2. After being released by the scheduler 104, in block 201, the instruction threads are loaded into the pipeline. In decision block 202, when a thread stalls, it is determined whether the stall is due to a dependent operation needed by the thread. If it is not (e.g., to address some execution latencies), control passes to block 204 where the thread completes execution through the pipeline. *If the stall is due to a dependent data operation, control passes to decision block 203 to determine if the data can be retrieved from memory either in the L1 cache or L2 cache, rather than from external memories. If it is found in the L1 cache or L2 cache, then control passes to block 204 to await return of data and continue execution through the pipeline. If it is not found in the L1 cache or L2 cache, control shifts to block 205 where the thread is flagged as a stall-miss-flush. Control then passes to block 206 where the exception and retirement logic 107 reads the flag and re-steers the thread to the front end and eventually back to the scheduler 104. The scheduler 104, in block 207, awaits a data return indication from the pipeline control logic 106 before returning control to block 201 to load the threads into the execution pipelines.* Likewise, if the thread does not stall, it continues through the pipeline for execution in a normal manner. One skilled in the art will appreciate that the amount of delay that is unacceptable to cause the thread to be flagged as a stall-miss-flush may be modified (e.g., only flag the thread as such if the dependent data is not in the L1 cache alone) (*emphasis added).*

As disclosed in the section above, the flushing of an instruction when data is to be loaded from the memory device in order to execute an instruction is specifically recited in independent claim 1. However, neither reference teaches, suggest or discloses such limitations anywhere in their disclosures. Hennessey discloses the flushing of instructions generally, but again not the flushing of an instruction when data is to be loaded from the memory device in order to execute an instruction. Additionally, Applicants respectfully submit that the Office Action's naked hypothetical application of Hennessey to Parady without any specific disclosure from either reference that reflects the actual claimed limitations does not suffice as a teaching, suggestion or disclosure and is insufficient to support a 35 U.S.C. 103(a) rejection. In order for a 103(a) rejection to succeed, each and

every limitation of independent claim 1 must be in the cited references. Since each and every limitation is not found in the cited references, the 103(a), claim 1 is allowable and the 103(a) rejection should be withdrawn.

In addition and in the alternative, Applicants respectfully submit that there is no suggestion or motivation to combine Parady and Hennessey beyond the impermissible use of hindsight. Applicants submit that a *prima facie* case of obviousness has not been made. The MPEP requires that the references must suggest making the combinations. MPEP §2141.01 (citing Hodosh v. Block Drug Co., Inc.); §706.02(j) (the initial burden is on the examiner to provide a convincing line of reasoning with explicit or implicit suggestions to combine references).

Merely stating that it would have been obvious for a person of ordinary skill in the art to combine references, without pointing to a specific hint or suggestion to combine, has been rejected by the Federal Circuit, as an invalid basis of rejection under 35 U.S.C. §103. *In re Lee*, 277 F.3d 1338, 1343 (Fed. Cir. 2002)(the court held that rejecting a conclusory statement that it would have been obvious to combine the references without evidence of a teaching, motivation, or suggestion to select and combine the references, citing numerous case); *In re Dembiczak*, 175 F.3d 994,999 (Fed. Cir. 1999) ("Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references.") In this case, the Office Action has taken the concept of "flush" disclosed in Hennessey and applied it in an ad hoc fashion to form the basis of its rejection. However, in addition to the arguments made above, there is no teaching, suggestion or motivation to combine to be found in the references that adequately form the basis of a proper 35 U.S.C. §103(a) rejection of independent claim 1. Independent

claims 5, 10, and 16 contain substantively similar limitations and therefore are also allowable for similar reasons. Claims 2-4, 6-9, 11-15 and 17-21 depend from allowable independent claims 1, 5, 10 and 16, and therefore are in condition for allowance as well.

For at least the above reasons, Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments to Deposit Account No. **11-0600**.

Respectfully submitted,

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